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#### **CMOS Design and Performance Analysis of Ring Oscillator ...**

Technology," International Journal of Computer Applications, Vol 83, no 15, pp 31-35, December 2013 [4] Manoj Kumar, Sandeep Kumar Arya and Sujata Pandey, "Voltage Controlled Ring Oscillator Design with Novel 3 Transistors XNOR/XOR Gates," and Conferences Dr Mehra has gScientific Research

#### **International journal of computer science & information ...**

International journal of computer science & information Technology (IJCSIT) Vol2, No5, October 2010 126 O (c) Figure1 Level shifter circuits (a) Conventional (b) Single supply (c) Contention

#### **LIST OF BOOKS/TEXT BOOKS WRITTEN BY FACULTY MEMBERS**

6 "VLSI Technology" by Sujata Pandey , Dhanpat Rai publishers, 2005 7 "Essential of Experimental Engineering Chemistry ", (Second edition, 2006)

Shashi Chawla, Dhanpat Rai & Co 8 "Theory and Practicals of Engineering Chemistry, (First edition, 2008) Shashi Chawla, Dhanpat Rai & Co 9

### **Design of Efficient XTEA Using Verilog - IJSRP**

Design of Efficient XTEA Using Verilog Shweta Gaba, Iti Aggarwal, Dr Sujata Pandey Electronics and Communication Engineering, Amity School of Engineering and Technology, Amity University, India Abstract- In this age of viruses and hackers of electronic eavesdropping and ...

### **Single bit full adder design using 8 transistors with ...**

Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate Sandeep K Arya 1 and Sujata Pandey 2 Guru Jambheshwar University of Science & Technology, Hisar, 125

### **Vipul Bhatnagar faculty profile**

1) Vipul Bhatnagar, Chandani Attri, Sujata Pandey, "Optimization of row decoder for 128x128 6T SRAMs", Proc of IEEE International Conference on VLSI Systems, Architecture, Technology & Applications , Bengaluru 2015 2) Vipul Bhatnagar, Sujata Pandey and Pradeep Kumar, "Analysis and implementation of

### **High Speed Level Shifter Design for Low Power Applications ...**

IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 2, In this section as a comparative analysis using 45nm Cadence GSDK technology the conventional level Shweta Pandey, "Level Shifter Design for Low Power Applications",

### **A Novel 3 Transistor XOR Gate Based Full Adder Design for ...**

Symposium on VLSI, pp 380-383, Feb 1999 [7] Manoj Kumar, Sandeep K Arya and Sujata Pandey, " Single bit Full adder design using 8 transistors with novel 3 transistors XNOR gate" International Journal of VLSI design & communication Systems, Vol2, no4, December 2011

### **ON THE MODELING OF DUAL-MATERIAL DOUBLE-GATE FULLY ...**

MATERIAL DOUBLE-GATE FULLY-DEPLETED SILICON-ON-INSULATOR MOSFET" being submitted by Alok Kumar Kushwaha to the National Institute of Technology Kurukshetra, Deemed University, Kurukshetra for the award of the degree of Doctor of Philosophy is a record of bonafide research work carried out by him

### **Design and Implementation of 4-bit Array Multiplier for ...**

High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design," in International Journal of VLSI design & Communication Systems (VLSICS) Vol3, No2, April 2012 [6] Manoj Kumar, Sandeep K Arya and Sujata Pandey, Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate in

### **IC-TELCON - Thakur College of Engineering and Technology**

engineering and technology hello\_yashpatel@yahoo.com Mr Rahul Kumar Jha Dept of Electronics Thakur college of engineering and technology rahuljha0609@gmail.com Mrs Sujata Alegavi Dept of Electronics Thakur college of engineering and technology sujatadubal@thakureducation.org Abstract -Livestock Management is a laborious task as the

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International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-2, Issue-1, March 2013 204 Abstract—Most of the VLSI circuits used adders as a crucial portion, since they form the base element of all arithmetic

### **CONFERENCE PAPERS 1. on Solid State Devices and Circuits in**

Technology and Science (ICCTS 2014) organized by IACSIT held in the Sarawak, Malaysia on 7-8, June, 2014) 22 AKGupta, SGovinda, " Design of low

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voltage rail to rail voltage to frequency converters for portable applications" Proceedings of the National Conference on VLSI, Signal Processing and **Power Optimization of Communication System Using Clock ...**

Power Optimization of Communication System Using Clock Gating Technique Kanika Sahni Kiran Rawat Sujata Pandey Ziauddin Ahmad Amity University Noida Uttar Pradesh, India Amity University Noida Uttar Pradesh, India This is the main task for the VLSI engineers and ...

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Adder Circuits, International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011 [9] Manoj Kumar, Sandeep K Arya and Sujata Pandey, Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate, International Journal of VLSI design & Communication Systems (VLSICS) Vol2, No4, December 2011

#### **Design and Implementation of a 4:2 Compressor Design with ...**

Most of the VLSI circuits used adders as a crucial portion, since they form the base widely used semiconductor technology used in the transistors It uses both NMOS (negative Sandeep K Arya, Sujata Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," International Journal of

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Manoj Kumar, Sandeep K Arya, and Sujata Pandey Low Power Voltage Controlled Ring Oscillator Design with Substrate Biasing International Journal of Information and Electronics Engineering, Vol 2, No 2, March 2012 156